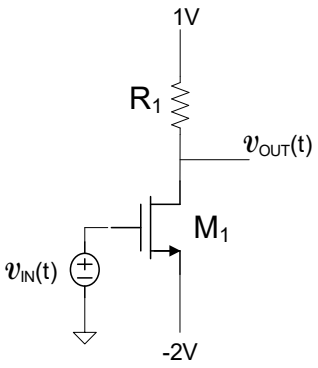
EE 330
Homework 11
Fall 2024 Due Friday November 8 at noon

Characteristics for an SCR and for a Triac are appended at the end of this assignment. Use these characteristics when solving the problems involving Thyristors. Unless specified to the contrary, assume all n-channel MOS transistors have model parameters $\mu_n C_{OX} = 250\mu A/V^2$,$V_{Tn} = 0.4V$, and $\lambda=0$, all p-channel transistors have model parameters $\mu_p C_{OX} = \mu_n C_{OX}/3$,$V_{Tp}= -0.4V$, and $\lambda=0$, and all JFET devices are from a process with $I_{DSSn0}= 100\mu A$, $I_{DSSp0}= 30\mu A$,$V_{Pp}=1V$, $V_{Pn}=-1V$, and , $\lambda=0$.

Problem 1 Consider the following circuit where $R_1=10K$. Size the device so that the amplifier has a voltage gain of -3.

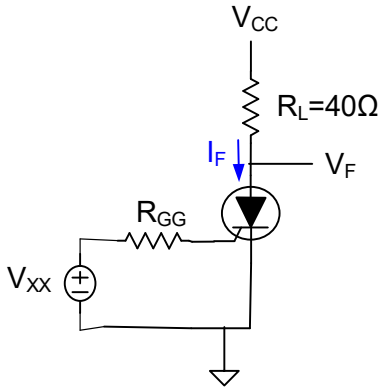


Problem 2 A circuit using an SCR that is rated at current levels of 10A is shown below. Relevant parameters from the datasheet for this device are appended at the end to this assignment. Assume the voltage V_{CC} is fixed at 50V and that the SCR is initially off.

a) If V_{XX} is increased to 12V to turn on the SCR, what is the maximum value of R_{GG} that can be used if the SCR must turn on for 0C<T<80C.

b) What will be the static power dissipation in the Anode when it is ON?

c) What will be the static power dissipation in the Gate if the gate signal V_{XX} remains at 12V and the value determined in part a) is used for R_{GG}?

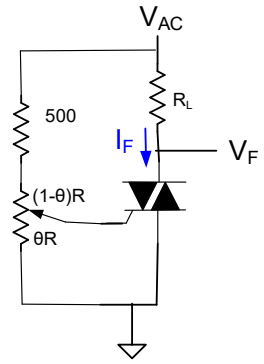


Problem 3 Assume the potentiometer in the following circuit has a full range value of R=500Ω, R_L=20Ω, and V_{AC}=80sin(2π60t). Assume the device is operating at a temperature of 25C and that it is characterized by the parameters given at the end of this assignment.

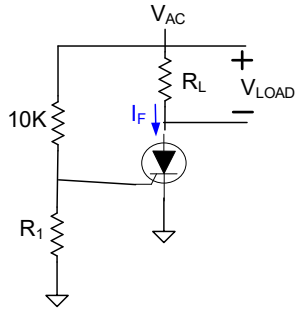
a) Determine $V_F(t)$ if θ=0.1

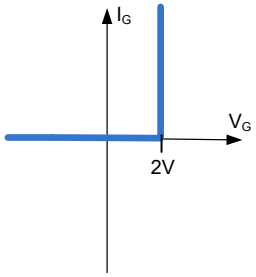
b) Determine the average power dissipation in the Triac for the value of θ given in part a)

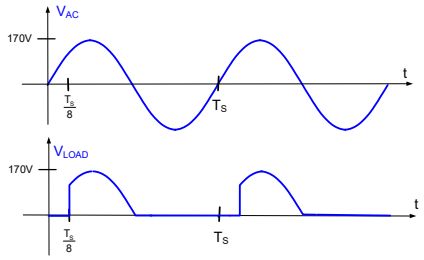
c) Which quadrant or quadrants are used to trigger the triac in this circuit?



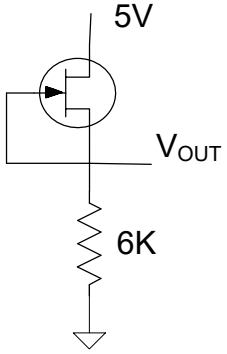
Problem 4 Consider the following circuit. The waveforms V_{AC} is the 60Hz line voltage. Assume the SCR has a gate trigger voltage of 2Vand that the relationship between the gate current and the gate voltage of the SCR is as shown on the I_G:V_G plot on the right. Size the resistor R_1 so that the SCR turns on at T_S/8, T_S +T_S/8, 2T_S +T_S/8,…. as shown below for two periods of the V_{LOAD} waveform. The time T_S is the period of the 60 Hz AC line voltage.







Problem 5 Assume the JFET in the following circuit has parameters I_{DSS}=100uA and V_P = -1V. Determine the output voltage.



Problem 6

Assume the drain current of a p-channel JFET is given by the expression

$$I_D = \begin{cases} 0 & V_{GS} > V_P \\ -\dfrac{2I_{DSSp0}W}{V_p^2 L}\left(V_{GS} - V_P - \dfrac{V_{DS}}{2}\right)V_{DS} & -0.3 < V_{GS} < V_P \quad V_{GS} + 0.3 > V_{DS} > V_{GS} - V_P \\ -\dfrac{I_{DSSp0}W}{L}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2 (1 - \lambda V_{DS}) & -0.3 < V_{GS} < V_P \quad V_{DS} < V_{GS} - V_P \end{cases}$$

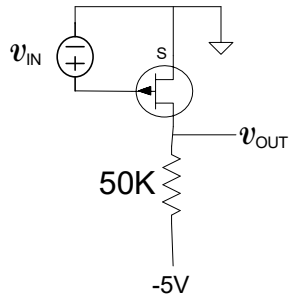
where the parameter I_{DDSp0} is related to the parameter I_{DDSp} that is often given in the model for a JFET by the expression

$$I_{DSSp} = \frac{W}{L} I_{DSSp0}$$

Develop a small-signal model of the JFET when operating in the saturation region.

Problem 7

Using the small-signal model of the JFET developed in the previous problem and the model parameters given at the top of this assignment, determine the operating point and small-signal voltage gain of the following circuit if W=10μm and L=15μm.

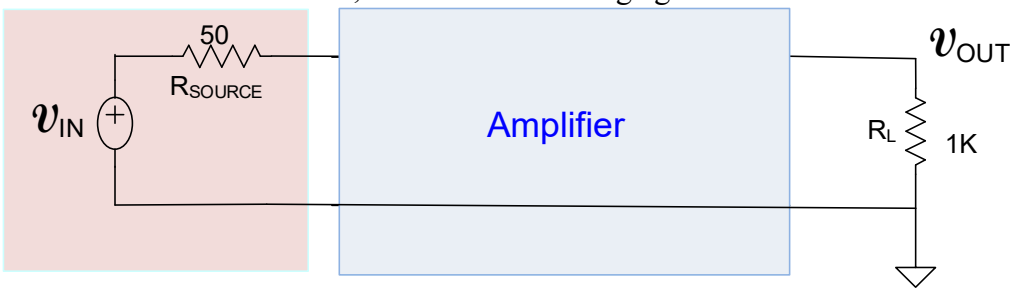


Problem 8 Consider a two-port amplifier with a common terminal between the input and the output characterized by the parameters $y_{11}=10^{-4}$ A/V $y_{21}=-10$ A/V and $y_{22}=0.1$A/V.

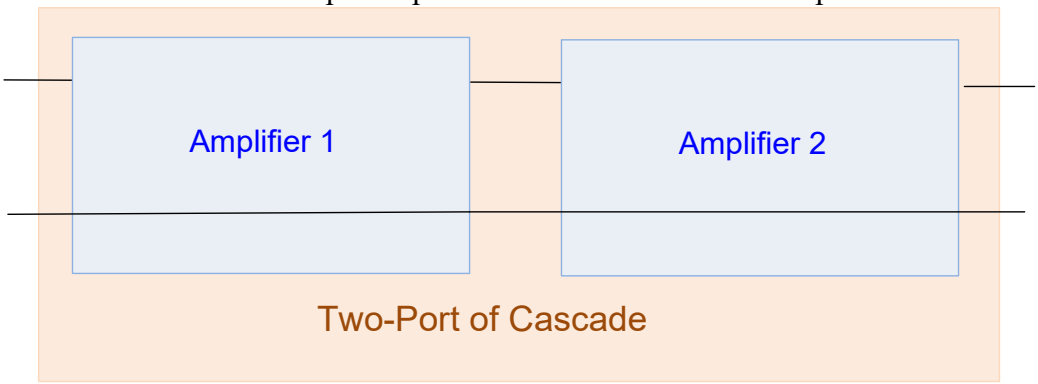
a) Is this amplifier unilateral ?

b) Express the small signal two-port model of this amplifier in terms of the small-signal amplifier parameters R_{IN}, R_{OUT}, A_V, and A_{VR}.

c) If this amplifier is driven by a voltage source with 50Ω source impedance and loaded with a 1KΩ resistor, determine the voltage gain.



d) If two of these amplifiers are cascaded, they also form a two-port amplifier. Determine the amplifier parameters for the cascaded amplifiers.



Problem 9-10 Implement a four-bit full adder with active low enable pin using Verilog. When the adder is disabled, all outputs should be low. Design a testbench proving function using Verilog. Submit module code, testbench code, and Modelsim waveforms.

SCR Specifications:

I_{DRM} and I_{RRM} — Peak off-state current at V_{DRM} and V_{RRM}

I_{GT} — DC gate trigger current V_D = 6 V dc; R_L = 100 Ω

I_{GM} — Peak gate current

I_H — DC holding current; initial on-state current = 20 mA

I_T — Maximum on-state current

V_{DRM} and V_{RRM} — Repetitive peak off-state forward and reverse voltage

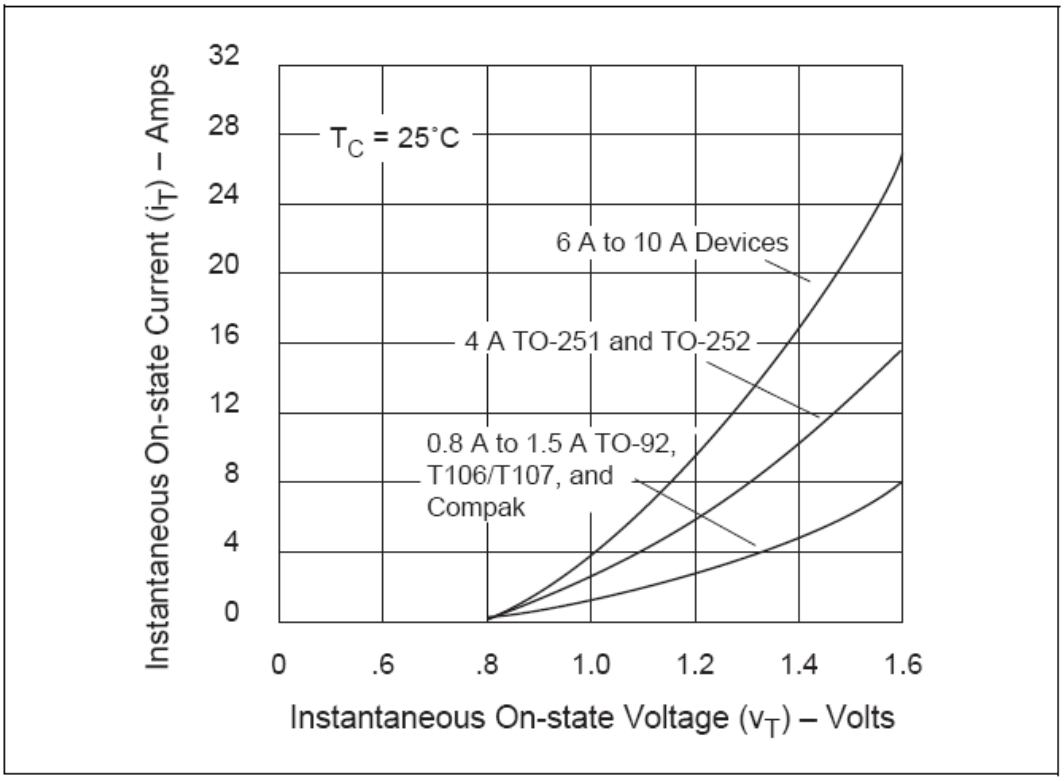
V_{GRM} — Peak reverse gate voltage

V_{GT} — DC gate trigger voltage; V_D = 6 V dc; R_L = 100 Ω

V_{TM} — Peak on-state voltage

I_T		V_{DRM} & V_{RRM}	I_{GT}	I_{DRM} & I_{RRM}		V_{TM}
Amps				μAmps		
$I_{T(RMS)}$	$I_{T(AV)}$	Volts	μAmps	T_C = 25 °C	T_C = 110 °C	Volts
MAX	MAX	MIN	MAX	MAX	MAX	MAX
10	**6.4**	**400**	**200**	**5**	**250**	**1.6**

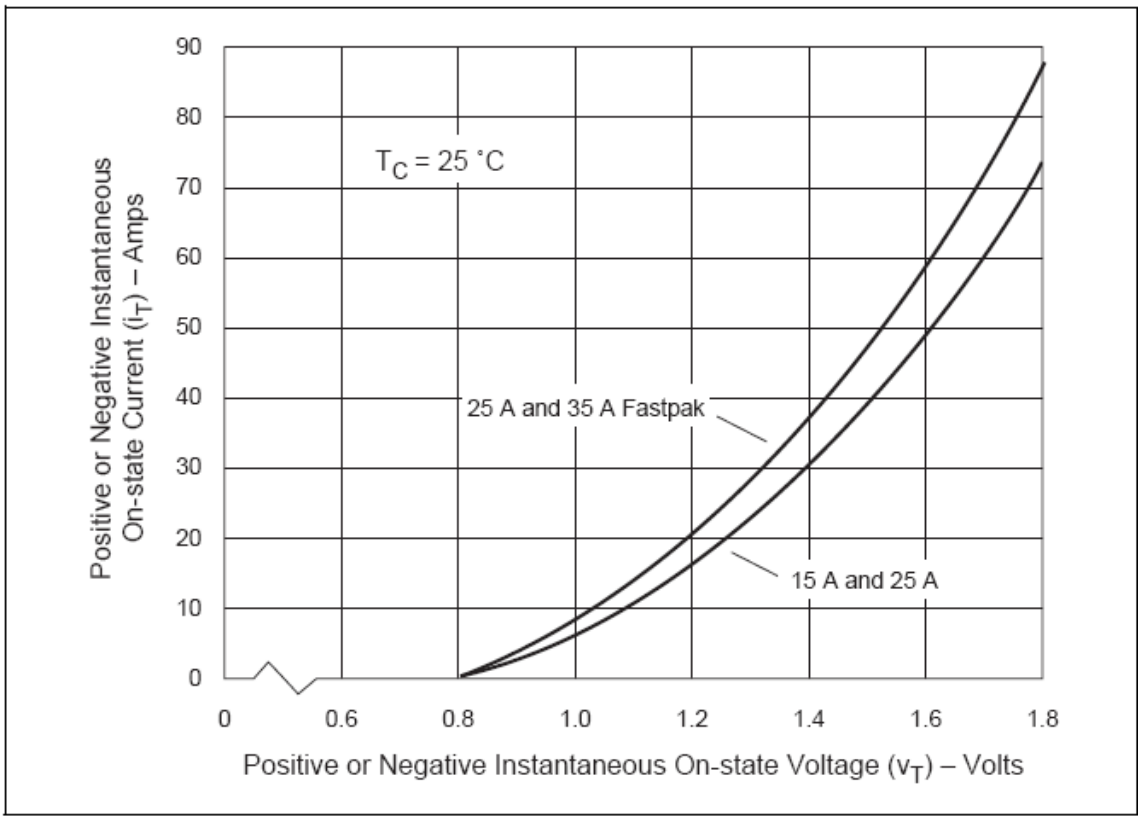
V_{GT}			I_H	I_{GM}	V_{GRM}	P_{GM}
Volts						
T_C = -40 °C	T_C = 25 °C	T_C = 110 °C	mAmps	Amps	Volts	Watts
MAX			MAX		MIN	
1	**0.8**	**0.25**	**6**	**1**	**6**	**1**

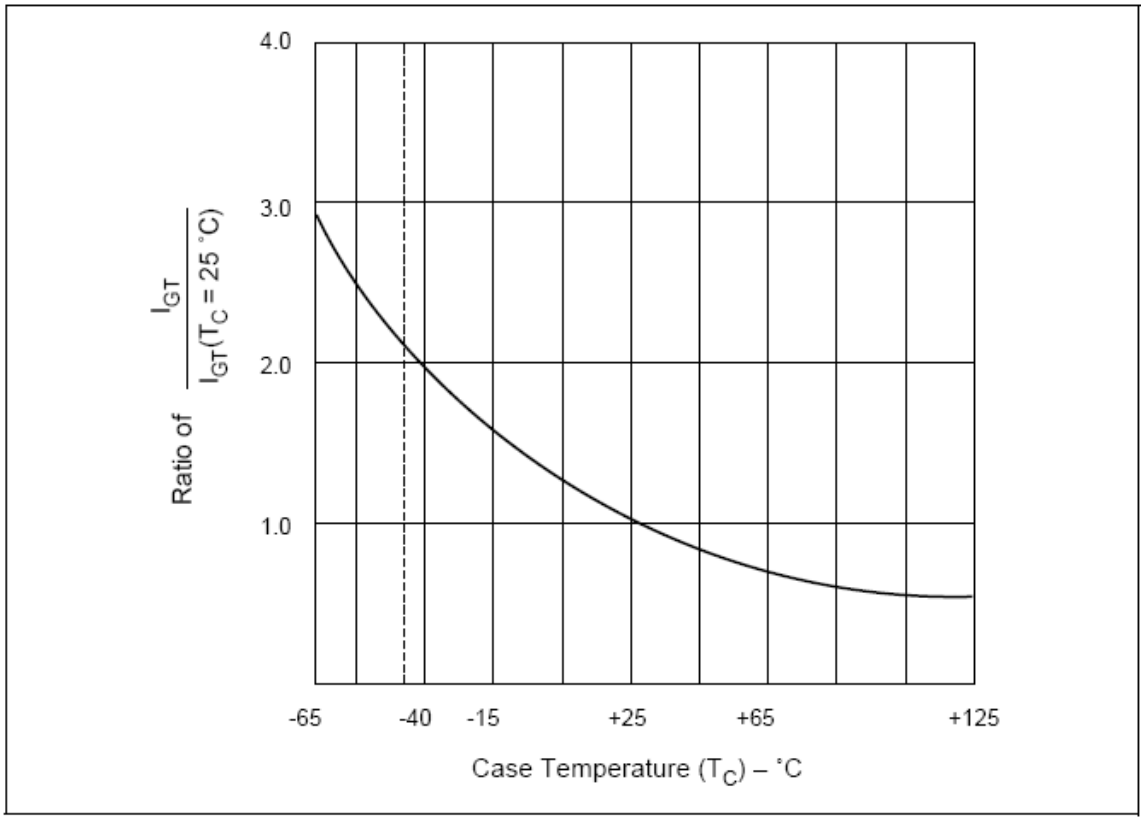

Instantaneous On-state Current (i_T) – Amps
32
28
24
20
16
12
8
4
0
T_C = 25°C
6 A to 10 A Devices
4 A TO-251 and TO-252
0.8 A to 1.5 A TO-92,
T106/T107, and
Compak
0
.6
.8
1.0
1.2
1.4
1.6
Instantaneous On-state Voltage (v_T) – Volts

TRIAC Specifications

V_{DRM}	I_{GT}					I_{DRM}		
	mAmps					mAmps		
Volts	QI	QII	QIII	QIV	QIV	T_C = 25 °C	T_C = 100 °C	T_C = 125 °C
MIN	MAX				TYP	MAX		
400	**50**	**50**	**50**			**0.05**	**0.5**	**2**

V_{TM}	V_{GT}	I_H	I_{GTM}	P_{GM}	$P_{G(AV)}$
Volts	Volts				
T_C = 25 °C	T_C = 25 °C	mAmps	Amps	Watts	Watts
1.6	**2.5**	**70**	**2**	**20**	**0.5**




4.0
3.0
2.0
1.0
Ratio of $\frac{I_{GT}}{I_{GT}(T_C = 25\ ^\circ C)}$
-65
-40
-15
+25
+65
+125
Case Temperature (T_C) – °C

Bipolar Process Characteristics

Parameter	Typical	Tolerance[b]	Units
Resistance and resistivity			
Substrate resistivity	16	±25%	Ω · cm
n^+ buried collector diffusion	17	±35%	Ω / □
Epitaxial layer	1.6	±20%	Ω · cm
p-base diffusion	160	±20%	Ω / □
p-resistive diffusion (optional)	1500	±40%	Ω / □
n^+ emitter diffusion	4.5	±30%	Ω / □
Metal	0.003		Ω / □
Contacts ($3\mu \times 3\mu$)	<4		Ω
Metal-n^+ emitter (contact plus series resistance to BE junction)	<1		Ω
Metal-p-base[c] (contact plus series resistance)	70		Ω
Metal-Epitaxial[d] (contact plus series resistance to BC junction)	120		Ω
Breakdown voltages, leakage currents, migration currents, and operating conditions			
Reverse breakdown voltages			
n^+ emitter to p-base	6.9	±50 mV	V
p-base to epitaxial	70	±10	V
Epitaxial to substrate	>80		V
Maximum operating voltage	40		V
Substrate leakage current	0.16		fA/μ^2
Maximum metal current density	0.8		mA/μ width
Maximum device operating temperature (design)	125		°C
Maximum device operating temperature (physical)	225		°C
Capacitances			
Metal to epitaxial	0.022	±30%	fF/μ^2
Metal to p-base diffusion	0.045	±30%	fF/μ^2
Metal to n^+ emitter diffusion	0.078	±30%	fF/μ^2
n^+ buried collector to substrate (junction, bottom)	0.062	±30%	fF/μ^2
Epitaxial to substrate (junction, bottom)	0.062	±30%	fF/μ^2
Epitaxial to substrate (junction, sidewall)	1.6	±30%	fF/μ perimeter
Epitaxial to p-base diffusion (junction, bottom)	0.14	±30%	fF/μ^2
Epitaxial to p-base diffusion (junction, sidewall)	7.9	±30%	fF/μ perimeter
p-base diffusion to n^+ emitter diffusion (junction, bottom)	0.78	±30%	fF/μ^2
p-base diffusion to n^+ emitter diffusion (junction, sidewall)	3.1	±30%	fF/μ perimeter

	Dimension
1. n^+ buried collector diffusion (Yellow, Mask #1)	
1.1 Width	3λ
1.2 Overlap of p-base diffusion (for vertical npn)	2λ
1.3 Overlap of n^+ emitter diffusion (for collector contact of vertical npn)	2λ
1.4 Overlap of p-base diffusion (for collector and emitter of lateral pnp)	2λ
1.5 Overlap of n^+ emitter diffusion (for base contact of lateral pnp)	2λ
2. Isolation diffusion (Orange, Mask #2)	
2.1 Width	4λ
2.2 Spacing	24λ
2.3 Distance to n^+ buried collector	14λ
3. p-base diffusion (Brown, Mask #3)	
3.1 Width	3λ
3.2 Spacing	5λ
3.3 Distance to isolation diffusion	14λ
3.4 Width (resistor)	3λ
3.5 Spacing (as resistor)	3λ
4. n^+ emitter diffusion (Green, Mask #4)	
4.1 Width	3λ
4.2 Spacing	3λ
4.3 p-base diffusion overlap of n^+ emitter diffusion (emitter in base)	2λ
4.4 Spacing to isolation diffusion (for collector contact)	12λ
4.5 Spacing to p-base diffusion (for base contact of lateral pnp)	6λ
4.6 Spacing to p-base diffusion (for collector contact of vertical npn)	6λ
5. Contact (Black, Mask #5)	
5.1 Size (exactly)	4λ × 4λ
5.2 Spacing	2λ
5.3 Metal overlap of contact	λ
5.4 n^+ emitter diffusion overlap of contact	2λ
5.5 p-base diffusion overlap of contact	2λ
5.6 p-base to n^+ emitter	3λ
5.7 Spacing to isolation diffusion	4λ

6. Metalization (Blue, Mask #6)	
6.1 Width	2λ
6.2 Spacing	2λ
6.3 Bonding pad size	$100\ \mu \times 100\ \mu$
6.4 Probe pad size	$75\ \mu \times 75\ \mu$
6.5 Bonding pad separation	$50\ \mu$
6.6 Bonding to probe pad	$30\ \mu$
6.7 Probe pad separation	$30\ \mu$
6.8 Pad to circuitry	$40\ \mu$
6.9 Maximum current density	$0.8\ \text{mA}/\mu$ width
7. Passivation (Purple, Mask #7)	
7.1 Minimum bonding pad opening	$90\ \mu \times 90\ \mu$
7.2 Minimum probe pad opening	$65\ \mu \times 65\ \mu$

CMOS Process Characteristics

Process parameters for a typical[a] p-well CMOS process

	Typical	Tolerance[b]	Units
Square law model parameters			
V_{T0} (threshold voltage)			
n-channel (V_{TN0})	0.75	± 0.25	V
p-channel (V_{TP0})	−0.75	± 0.25	V
K'(conduction factor)			
n-channel	24	± 6	$\mu A/V^2$
p-channel	8	± 1.5	$\mu A/V^2$
γ(body effect)			
n-channel	0.8	± 0.4	$V^{1/2}$
p-channel	0.4	± 0.2	$V^{1/2}$
λ(channel length modulation)			
n-channel	0.01	± 50%	V^{-1}
p-channel	0.02	± 50%	V^{-1}
ϕ(surface potential)			
n- and p-channel	0.6	± 0.1	V
Process parameters			
μ (channel mobility)			
n-channel	710		$cm^2/(V \cdot s)$
p-channel	230		$cm^2/(V \cdot s)$
Doping[c]			
n^+ active	5	±4	$10^{18}/cm^3$
p^+ active	5	±4	$10^{17}/cm^3$
p-well	5	±2	$10^{16}/cm^3$
n-substrate	1	±0.1	$10^{16}/cm^3$

Physical feature sizes			
T_{ox} (gate oxide thickness)	500	± 100	Å
Total lateral diffusion			
n-channel	0.45	± 0.15	μ
p-channel	0.6	± 0.3	μ
Diffusion depth			
n^+ diffusion	0.45	± 0.15	μ
p^+ diffusion	0.6	± 0.3	μ
p-well	3.0	± 30%	μ
Insulating layer separation			
POLY I to POLY II	800	± 100	Å
Metal 1 to Substrate	1.55	± 0.15	μ
Metal 1 to Diffusion	0.925	± 0.25	μ
POLY I to Substrate (POLY I on field oxide)	0.75	± 0.1	μ
Metal 1 to POLY I	0.87	± 0.7	μ
Metal 2 to Substrate	2.7	± 0.25	μ
Metal 2 to Metal I	1.2	± 0.1	μ
Metal 2 to POLY I	2.0	± 0.07	μ
Capacitances[d]			
C_{OX} (gate oxide capacitance, n- and p-channel)	0.7	±0.1	fF/μ^2
POLY I to substrate, poly in field	0.045	±0.01	fF/μ^2
POLY II to substrate, poly in field	0.045	±0.01	fF/μ^2
Metal 1 to substrate, metal in field	0.025	±0.005	fF/μ^2
Metal 2 to substrate, metal in field	0.014	±0.002	fF/μ^2
POLY I to POLY II	0.44	±0.05	fF/μ^2
POLY I to Metal 1	0.04	±0.01	fF/μ^2
POLY I to Metal 2	0.039	±0.003	fF/μ^2
Metal 1 to Metal 2	0.035	±0.01	fF/μ^2
Metal 1 to diffusion	0.04	±0.01	fF/μ^2
Metal 2 to diffusion	0.02	±0.005	fF/μ^2
n^+ diffusion to p-well (junction, bottom)	0.33	±0.17	fF/μ^2
n^+ diffusion sidewall (junction, sidewall)	2.6	±0.6	fF/μ
p^+ diffusion to substrate (junction, bottom)	0.38	±0.12	fF/μ^2
p^+ diffusion sidewall (junction, sidewall)	3.5	±2.0	fF/μ
p-well to substrate (junction, bottom)	0.2	±0.1	fF/μ^2
p-well sidewall (junction, sidewall)	1.6	±1.0	fF/μ
Resistances			
Substrate	25	±20%	Ω-cm
p-well	5000	±2500	Ω/□
n^+ diffusion	35	±25	Ω/□
p^+ diffusion	80	±55	Ω/□
Metal	0.003	±25%	Ω/□
Poly	25	±25%	Ω/□
Metal 1–Metal 2 via (3 μ × 3 μ contact)	<0.1		Ω
Metal 1 contact to POLY I (3 μ × 3 μ contact)	<10		Ω
Metal 1 contact to n^+ or p^+ diffusion (3 μ × 3 μ contact)	<5		Ω

		Dimensions	
		Microns	**Scalable**
1.	p-well (CIF Brown, Mask #1[a])		
1.1	Width	5	4λ
1.2	Spacing (different potential)	15	10λ
1.3	Spacing (same potential)	9	6λ
2.	Active (CIF Green, Mask #2)		
2.1	Width	4	2λ
2.2	Spacing	4	2λ
2.3	p^+ active in n-subs to p-well edge	8	6λ
2.4	n^+ active in n-subs to p-well edge	7	5λ
2.5	n^+ active in p-well to p-well edge	4	2λ
2.6	p^+ active in p-well to p-well edge	1	λ
3.	Poly (POLY I) (CIF Red, Mask #3)		
3.1	Width	3	2λ
3.2	Spacing	3	2λ
3.3	Field poly to active	2	λ
3.4	Poly overlap of active	3	2λ
3.5	Active overlap of poly	4	2λ
4.	p^+ select (CIF Orange, Mask #4)		
4.1	Overlap of active	2	λ
4.2	Space to n^+ active	2	λ
4.3	Overlap of channel[b]	3.5	2λ
4.4	Space to channel[b]	3.5	2λ
4.5	Space to p^+ select	3	2λ
4.6	Width	3	2λ

7.	Via [e] (CIF Purple Hatched, Mask #C1)			
	7.1	Size, exactly	3 × 3	2λ × 2λ
	7.2	Separation	3	2λ
	7.3	Space to poly edge	4	2λ
	7.4	Space to contact	3	2λ
	7.5	Overlap by metal 1	2	λ
	7.6	Overlap by metal 2	2	λ
	7.7	Space to active edge	3	2λ
8.	Metal 2 (CIF Orange Hatched, Mask #C2)			
	8.1	Width	5	3λ
	8.2	Spacing	5	3λ
	8.3	Bonding pad size	100 × 100	100 μ × 100 μ
	8.4	Probe pad size	75 × 75	75 μ × 75 μ
	8.5	Bonding pad separation	50	50 μ
	8.6	Bonding to probe pad	30	30 μ
	8.7	Probe pad separation	30	30 μ
	8.8	Pad to circuitry	40	40 μ
	8.9	Maximum current density	0.8 mA/μ	0.8 mA/μ
9.	Passivation[f] (CIF Purple Dashed, Mask #8)			
	9.1	Bonding pad opening	90 × 90	90 μ × 90 μ
	9.2	Probe pad opening	65 × 65	65 μ × 65 μ
10.	Metal 2 crossing coincident metal 1 and poly[g]			
	10.1	Metal 1 to poly edge spacing when crossing metal 2	2	λ
	10.2	Rule domain	2	λ
11.	Electrode (POLY II)[h] (CIF Purple Hatched, Mask #A1)			
	11.1	Width	3	2λ
	11.2	Spacing	3	2λ
	11.3	POLY I overlap of POLY II	2	λ
	11.4	Space to contact	3	2λ